DETAILED ACTION

1. This Final Office Action responds to Applicant's amendment filed 1/31/2011. Claims 36, 39, 41, 77 and 79 have been amended. Claims 36-45 and 71-79 are pending.

Response to Amendment

2. Applicant's arguments and claim amendments filed 1/31/2011 have been considered but are not persuasive. Applicable rejections are incorporated herein.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claim 39 is rejected** under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

5. Claim 39 depends from independent claim 36.

6. As best understood by the Examiner regarding claim 39 and claim 36 from which it depends, and Figs. 7-8 below for the present invention:

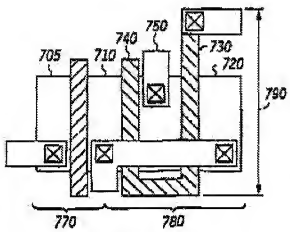


FIG. 7

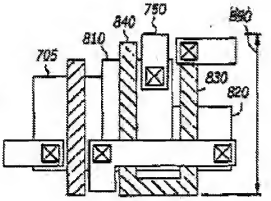


FIG. 8

7. A first logical device (Fig. 7) comprises a first transistor (Fig. 7 #780) and second transistor (Fig. 7 #770). The portion of the first transistor (Fig. 7 #730, transistor finger) extends in a first direction from the first logical device, and is reduced (Claim 36, lines 10-12, Fig. 8 #830). In response to the reduction of the portion of the first transistor, a "portion of the first logical device different from the portion of the first transistor", which the first logical device also comprises, is reshaped (Claim 36, lines 13-14, Fig. 7 # 740, transistor finger, Fig. 8 #840, resulting transistor finger).

8. The Examiner notes that as amended, claim 39, which depends from claim 36, claims wherein "the portion of the first logical device comprises a transistor finger *of a second transistor*". As exemplified above as taken from Figs. 7-8 and based on review of the Application specification, there is enablement for the portion of the first logical device (Fig. 7) to comprise "a second transistor finger of the first transistor" (Fig. 7 #740, Fig. 8 #840) **as in dependent claim 38**, but **not** for the first logical device (Fig. 7) to comprise "a transistor finger of a second transistor" reshaped in response to the

reshaping of a transistor finger of the first transistor **as in dependent claim 39.** If Applicant has intended for the limitation of claim 39 to refer to the transistor finger of second transistor (Fig. 7 #770), the Examiner notes that when comparing Fig. 7 to Fig. 8, there appears to be no change to said transistor finger.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. **Claims 36-45 and 71-79 are rejected** under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. **Pursuant to independent claim 36**, the limitation "the third portion (see line 21) lack proper antecedent basis. The Examiner suggests replacing "the third portion" with --the portion of the second transistor--.

12. **Pursuant to independent claim 36**, lines 6-9, it is unclear to the Examiner as to what is meant by "the portion of the first logical device different from the portion of the first transistor" which is later reshaped in lines 13-14.

13. Again referring to Figs. 7-8 below for the present invention:

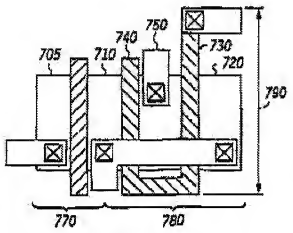


FIG. 7

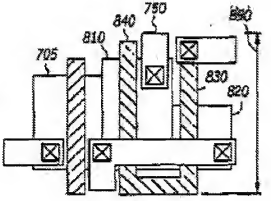


FIG. 8

14. A first logical device (Fig. 7) comprises a first transistor (Fig. 7 #780) and second transistor (Fig. 7 #770). The portion of the first transistor (Fig. 7 #730, transistor finger) extends in a first direction from the first logical device, and is reduced (Claim 36, lines 10-12, Fig. 8 #830). In response to the reduction of the portion of the first transistor, a "portion of the first logical device different from the portion of the first transistor", which the first logical device also comprises, is reshaped (Claim 36, lines 13-14, Fig. 7 # 740, transistor finger, Fig. 8 #840, resulting transistor finger).

15. Thus it is unclear to the Examiner as to how exactly "the portion of the first logical device" (Fig. 7 #740, Fig. 8 #840) can be "different from the portion of the first transistor" (Fig. 7 #730, Fig. 8 #830), when they actually make up the gate portion of the same first transistor (Fig. 7 #780).

16. Examiner suggests clarification with regards to what "the portion of the first logical device different from the portion of the first transistor" actually represents. Does the "portion of a first transistor" in claim 36, line 4, represent a first portion of a first

finger of the first transistor, and does the "portion of the first logical device different from the portion of the first transistor" in claim 36, lines 7-9, represent a second finger of the first transistor?

17. **Pursuant to independent claim 79,** lines 6-8, the limitation "the first logical device comprising...*a second portion*" is unclear. Second portion of what? Second portion of the first transistor? Second portion of the first logical device? If intended to refer to a second portion of the first logical device, the Examiner notes that there is no defining of the "first portion" of the first logical device in claim 79.

18. Claim 79 is similarly unclear with regards to the reasons above for claim 36, and should be similarly addressed by the Applicant.

19. **Pursuant to claim 79,** lines 5 and 9, "the first portion" lacks proper antecedent basis. Insert --of the first transistor-- after "the first portion" for proper antecedent basis.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. **Claims 36-41, 43-46, 71-75 and 77-79 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Shinomiya et al. (Shinomiya) (US 5,852,562) in view of Maziasz et al. (Maziasz) (US 6,209,123).

22. Shinomiya discloses

23. (Claims 36 and 79) A method comprising:

during compaction of a circuit layout determining at a computer device a first direction associated with the circuit layout (Shinomiya, Fig. 17 # S11, Col. 12, ll. 45-59, based on a determined cell row height; wherein Shinomiya discloses modification of a circuit layout through transistor folding/unfolding);

selecting at the computer device a portion of a first transistor in response to determining the portion of the first transistor extends outward in a first direction from a first logical device of the circuit layout (Shinomiya, Fig. 17 # S12, Fig. 19, Col. 13, ll. 7-37, wherein a big transistor may need to be folded during vertical compaction because of cell row height limitation), the first logical device (Shinomiya, Fig. 20 #41c) comprising when the portion of the first transistor is selected, the first transistor (Shinomiya, transistor Fig. 21 #400B and its right finger to be folded/reduced and transistor Fig. 20 # 400b are transformed versions of one another) and a portion of the first logical device, the portion of the first logical device different from the portion of the first transistor (Shinomiya, cell Fig. 21 #400B, left finger is a different portion than the right finger, but still a portion of the first logical device Fig. 20 #41c different than the right finger "portion" of the first transistor in Fig. 21 #400B) (note: Shinomiya is applied as best understood with respect to the 112 rejections of independent claims 36 and 79);

in response to selecting the portion of the first transistor, reshaping at the computer device the first transistor to reduce a size of the first logical device in the first direction (Shinomiya, Fig. 17 # S12, Fig. 19, Col. 13, ll. 7-37, wherein a big transistor is folded during vertical compaction because of cell row height limitation; wherein transistor Fig. 20 #400b of device Fig. 20 #41c represents a transformed transistor

version of Fig. 21 #400B reduced in a vertical direction, with the overall cell Fig. 20#41c being less in height than as in Fig. 21);

reshaping at the computer device the portion of the first logical device in response to reducing the size of the first logical device (Shinomiya, Fig. 17 # S12, Fig. 19, Col. 13, ll. 7-37, Col. 14, ll. 1-9, wherein a big transistor is folded during vertical compaction because of cell row height limitation, resulting in multiple transistor folds or fingers) (Shinomiya, wherein we see for example transistor (Fig. 20 #400b) of cell/device (Fig. 20 #41C) is reshaped through unfolding so that portions of transistor fingers are reallocated to other existing fingers of that transistor (Fig. 21 #400B) for compaction should a height allow it; as Shinomiya discloses wherein transistors may alternatively be folded as well as unfolded (Shinomiya, Col. 13, ll. 7-37), it is within the scope of Shinomiya that given a particular height requirement for cell row (Fig. 21 #40b), reallocation in part of a portion of the right finger of transistor Fig. 21 #400B to the left finger of Fig. 21 #400B would be sufficient should such an action satisfy the given particular height/spacing requirement and not cause any design errors; with the creation of new folds (Fig. 20 #400b) determined as necessary for smaller height requirements).

24. Shinomiya discloses either vertical or horizontal layout compaction through folding or unfolding of transistors (Shinomiya, Col. 13, ll. 61-67 – Col. 14, ll. 1-9 and 14-19, transistor folding or unfolding to adjust height and width, Col. 15, ll. 11-16, vertical or horizontal layout compaction) but does not explicitly disclose both horizontal and vertical compaction, and thus does not disclose the limitations of:

determining at the computer device a second direction associated with the circuit layout, the second direction different from the first direction;

selecting at the computer device a portion of a second transistor of the circuit layout in response to determining the portion of the second transistor extends outward in the second direction from a second logical device of the circuit layout, the second logical device comprising the second transistor;

in response to selecting the portion of the second transistor, reshaping at the computer device the portion of the second transistor to reduce a size of the second logical device in the second direction;

reshaping at the computer device a portion of the second logical device in response to reducing the size of the second logical device.

25. Maziasz discloses compaction of a design layout to meet height constraints, wherein for example after meeting a desired cell height through compaction in a Y direction, further compaction in an X direction (which is different than the Y direction) is then performed on the circuit layout (Maziasz, Col. 14, ll. 24-67 – Col. 15, ll. 1-2).

26. It would have been obvious to one of ordinary skill in the art to compact a layout design in both Y and X directions in order to provide for the most efficient area utilization possible (Maziasz, Col. 14, ll. 24-35).

27. The combination of Shinomiya in view of Maziasz further discloses:

28. (Claim 37) Wherein the portion of the first transistor comprises a first transistor finger (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

29. (Claim 38) Wherein the portion of the first logical device comprises a second transistor finger of the first transistor (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

30. (Claim 39) Wherein the portion of the first logical device comprises a transistor finger of a second transistor (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers; wherein Fig. 20 #400b and the transistor below it are transformed versions of Fig. 21 #400B and the transistor below in a configuration to meet height requirements for row Fig. 20 #41c) (Wherein as indicated in the rejection of claim 39 under 35 USC 112 above, there does not appear to be enablement for the first logical device to comprise "a transistor finger of a second transistor".).

31. (Claims 40) Wherein reshaping the portion of the first transistor comprises reducing a size of the first transistor finger (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

32. (Claims 41) Wherein reshaping the portion of the first transistor comprises removing the first transistor finger (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

33. (Claim 43) Reshaping the portion of the first logical device in response to reducing the size of the portion of first transistor (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

34. (Claims 44 and 45) Storing a first state associated with the circuit layout at the computer device in response to selecting the portion of the first transistor;

in response to reshaping the portion of the first transistor, determining if a size of the circuit layout has been reduced in the first direction (Maziasz, Fig. 9 and applicable text) (Shinomiya, Figs. 17 and 19 and applicable text); and

in response to determining the size of the circuit layout has not been reduced, restoring the circuit layout to the first state (Maziasz, Fig. 9 and applicable text, wherein compaction in a Y direction is first as there would be no reason to compact in the X direction following if the Y direction constraints are not yet met) (Shinomiya, Figs. 17 and 19 and applicable text) (wherein it is implicit in layout optimization that if a proposed solution does not meet cell height constraints it would not be a valid solution).

35. (Claim 71) Wherein the portion of the second transistor comprises a first transistor finger (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

36. (Claim 72) Wherein the portion of the second logical device comprises a second transistor finger of the first transistor (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

37. (Claim 73) Wherein the portion of the seconds logical device comprises a second transistor finger of the second transistor (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

38. (Claim 74) Wherein reshaping the portion of the second transistor comprises reducing a size of the second transistor finger (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

39. (Claim 75) Wherein reshaping the portion of the second transistor comprises removing the first transistor finger (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

40. (Claim 77) Wherein the portion of the second transistor comprises a first transistor finger (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

41. (Claim 78) Wherein reshaping the portion of the second transistor comprises reducing a size of the second transistor finger (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers)s.

42. **Claims 42 and 76 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Shinomiya et al. (Shinomiya) (US 5,852,562) in view of Maziasz et al. (Maziasz) (US 6,209,123), further in view of Wang, L. Y. et al. (Wang), "Topological cell compaction via transistor rotation", 1991, Circuits and Systems, Vol. 2, Pages 909-912.909-912.

43. Shinomiya in view of Maziasz discloses all of the elements of claim 36 from which claims 42 and 76 depend.

44. Shinomiya in view of Maziasz does not disclose:

a. (Claim 42) Wherein reshaping the portion of the first transistor comprises rotating the first transistor; and

b. (Claim 76) Wherein reshaping the portion of the second transistor comprises rotating the second transistor.

45. Wang discloses topological layout compaction inclusive of transistor rotation to change the layout topology (Wang, Page 910, Section 3).

46. It would have been obvious to one of ordinary skill in the art the addition of transistor rotation would provide for increased compaction options and flexibility for layout optimization.

Remarks

47. In light of Applicant's claim amendments filed 1/31/2011:

48. The previous objections to claims 39 and 77 have been removed.

49. The rejection of claims 36-45 and 71-79 under 35 U.S.C. 112, second paragraph, have been removed in part and maintained in part. New rejections of claims 36-45 and 71-79 under 35 U.S.C. 112, second paragraph have also been made (See rejections above).

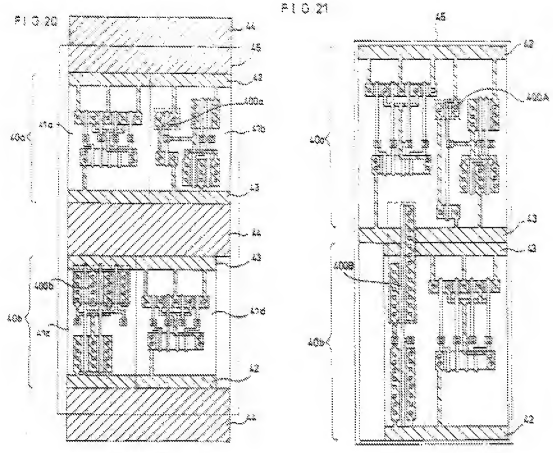
50. **Pursuant to claims 36 and 79**, Applicant argues that Shinomiya does not disclose a "first logical device, comprising, when the portion of the first transistor is selected, the first transistor and a portion of the first logical device, the portion of the first logical device different from the portion of the first transistor" because Shinomiya's fingers are not pre-existing at the time a first logical device is selected for reshaping (See Remarks, Page 7).

51. The Examiner is not persuaded.

52. Shinomiya discloses modification of a circuit layout through transistor folding/unfolding (Shinomiya, Fig. 17 # S12, Fig. 19, Col. 13, ll. 7-37, wherein a big

transistor may need to be folded during vertical compaction because of cell row height limitation; wherein a transistor may also be unfolded vertically).

53. Taking into consideration Figs. 20 and 21 of Shinmiya below:



54. We see wherein for example transistor (Fig. 20 #400b) of cell/device (Fig. 20 #41C) is reshaped through unfolding so that portions of transistor fingers are reallocated to other existing fingers of that transistor (Fig. 21 #400B) for compaction should a height allow it. As Shinomiya discloses wherein transistors may alternatively be folded as well as unfolded (Shinomiya, Col. 13, ll. 7-37), it is within the scope of Shinomiya that given a particular height requirement for cell (Fig. 21 #40b), the right finger of Fig. 21 #400B

may only need to be reallocated in part to the left finger of Fig. 21 #400B as opposed to creation of new folds (Fig. 20 #400b) should such an action satisfy the given particular height/spacing requirement and not cause any design errors.

55. **Regarding claim 39**, Applicant argues that Shinomiya does not disclose reshaping of a transistor finger of a different transistor in response to reducing the size of the first logical device.

56. The Examiner is not persuaded.

57. First of all, as amended, claim 39 is currently rejected (see rejections above) under 35 U.S.C. 112, first paragraph, as there does not appear to be enablement for the limitation wherein "the portion of the first logical device comprises a transistor finger of a second transistor".

58. As best understood by the Examiner regarding the claim limitations of claim 39 and in light of the rejection of claim 39 under 35 U.S.C. 112, first paragraph, Shinomiya discloses folding/unfolding of transistors as deemed for compaction; as the transistor of Fig. 20 #400b and the transistor below it are transformed versions of Fig. 21 #400B and the transistor below in a configuration to meet either height requirements for row Fig. 20 #41c, or perhaps horizontal compaction requirements (wherein Fig. 21 #400B and the transistor below it are both reduced versions of Fig. 20#400b and the transistor below it in the horizontal direction), Shinomiya discloses reshaping of transistor fingers of a first transistor and in response that of transistor fingers of a second transistor.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PATRICK SANDOVAL whose telephone number is (571)272-7973. The examiner can normally be reached on 8:00 am to 5:30 pm Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Patrick Sandoval/
Examiner, Art Unit 2825

/Jack Chiang/

Supervisory Patent Examiner, Art Unit 2825